

Memory characteristics of $\text{Al}_2\text{O}_3/\text{LaAlO}_3/\text{SiO}_2$ multilayer structures with tunnel oxide thickness variation

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Abstract Charge trap flash (CTF) memory devices are candidates to replace NAND flash devices. In this study, $\text{Pt}/\text{Al}_2\text{O}_3/\text{LaAlO}_3/\text{SiO}_2/\text{Si}$ multilayer structures with lanthanum aluminate charge traps were fabricated for non-volatile memory device applications. An aluminum oxide film was used as a blocking oxide for low power consumption in the program/erase operation and to minimize charge transport through the blocking oxide layer. The thickness of SiO_2 as tunnel oxide layer was varied from 30 to 50 Å. Thicknesses of oxide layers were confirmed by high resolution transmission electron microscopy (HRTEM) and all the samples showed amorphous structure. From the C - V measurement, a maximum memory window of 3.4 V was observed when tunnel oxide thickness was 40 Å. In the cycling test for reliability, the 30 Å tunnel oxide sample showed a relatively large memory window reduction by repeated program/erase operations due to the high electric field of ~ 10 MV/cm through tunnel oxide. The other samples showed less than 10% loss of memory window during 10^4 cycles.

Introduction

Currently, flash memory uses floating gate-type for charge storage. However, this structure using floating gate cannot be continuous scaling down in near future due to difficult manufacture processing (i.e., coupling ratio (ab)) and wide

threshold voltage (V_{th}) distribution. To solve these problems, stacked layer-type structure without floating gate was suggested. This structure calls charge trap flash (CTF).

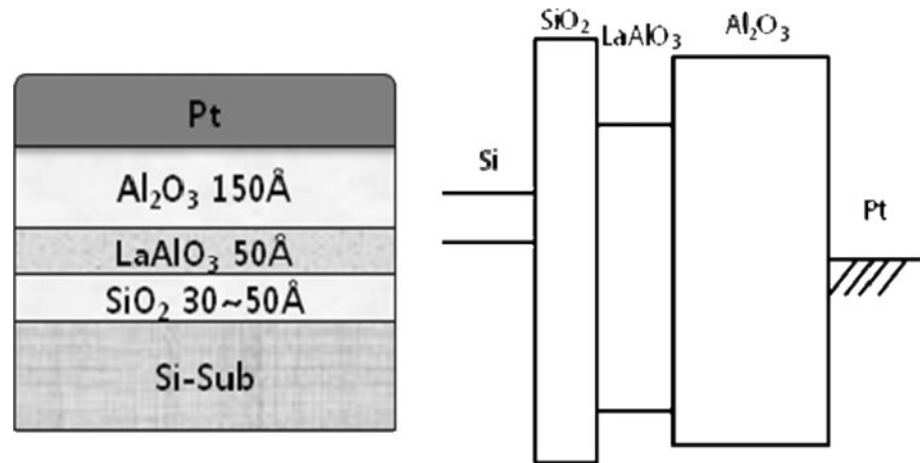
CTF memory has attracted increasing attention as a potential replacement of flash memory devices to resolve the problems such as low coupling ratio, mechanical instability, and data loss through the tunneling layer [1, 2]. SONOS (poly-Si/ $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$) is the most widely studied structure for CTF and exhibits low capacitance coupling and narrow threshold voltage distribution compared with nano-crystal memories [3, 4]. However, the high erase power and poor retention properties associated with SONOS need to be solved for conventional use [5, 6]. To solve these problems, many studies have been reported using other materials instead of Si_3N_4 and SiO_2 considering bandgap structures. Utilizing high- κ materials can reduce program and erase power consumption, and increasing the thickness of the blocking oxide can reduce leakage current through the blocking oxide [7–9]. In this study, the memory characteristics of an $\text{Al}_2\text{O}_3/\text{LaAlO}_3/\text{SiO}_2$ structure instead of the conventional $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$ (ONO) were investigated for CTF memory applications. In this structure, lanthanum aluminate between aluminum oxide and silicon oxide was utilized for charge storage to replace silicon nitride due to its lower conduction band offset [10]. Further, aluminum oxide was used as blocking oxide and Pt electrodes were used to minimize charge transport through the blocking oxide.

Experiments

We have fabricated three different multilayer structures with different tunnel oxide thicknesses. After a standard cleaning process for the n-type silicon (100) substrate and a

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Fig. 1 Schematic diagram of the Pt/Al₂O₃/LaAlO₃/SiO₂/Si multilayer structure and energy band diagram



native oxide removal process using a HF dipping process, the SiO₂ tunnel oxide was grown on the bare Si wafer by rapid thermal oxidation (RTO) at 850 °C in a dry O₂ atmosphere. The tunnel oxide thicknesses were 30, 40, and 50 Å. And then, a 50 Å LaAlO₃ charge trap layer on the tunnel oxide layer was deposited by metal–organic chemical vapor deposition (MOCVD), followed by 150 Å Al₂O₃ blocking oxide deposition. To deposit the charge trap layer, a La(tmhd)₃ tetraglyme adduct and Al(acac)₃ were utilized as precursors with a flow rate of 30 sccm for each gas. N₂ was used as a carrier gas, while for oxide formation, 100 sccm of O₂ was used. The substrate temperature was maintained at 350 °C during deposition for all films, and the working pressure was maintained at 5 torr (266.6 Pa). The overall structure and its band diagram are illustrated in Fig. 1.

Pt electrodes were deposited on the oxide multilayer by DC magnetron sputtering using a shadow mask. The thicknesses of the oxide layers were measured by ellipsometry (Gaertner L117, $\lambda = 632.8$ nm) and the overall structure was confirmed with high resolution transmission electron microscopy (HRTEM). Charge trapping properties were characterized by Fowler–Nordheim (F–N) tunneling with a C–V analyzer (HP 4280A, 1 MHz). The program and erase conditions were 5–13 V for 3–1000 ms, and –5 to –13 V for 3–1000 ms, respectively.

Results and discussion

Figure 2 shows a HRTEM image of the multilayer structure. The thicknesses of the tunneling oxide (SiO₂), high- κ trapping layer (LaAlO₃), and high- κ blocking oxide (Al₂O₃) were found to be 40, 50, and 150 Å, respectively. Diffraction patterns indicate all films were deposited in an amorphous state. Hence, leakage of stored charge through the grain boundary should be prevented.

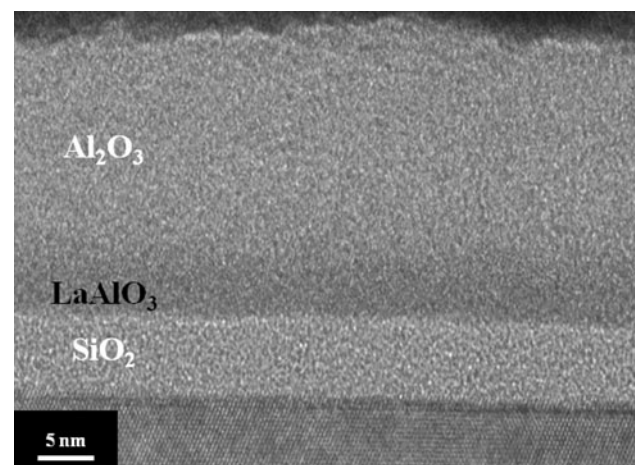


Fig. 2 HRTEM image of Al₂O₃ (top layer)/LaAlO₃ (middle layer)/SiO₂ (bottom layer)/Si structure and diffraction pattern

Figure 3 shows the threshold voltage (V_{th}) shift after various program pulses. In the program pulse and C–V sweep measurement, a maximum V_{th} shift was obtained in the case of 40 Å tunnel oxide. In the case of 30 Å tunnel oxide sample, a threshold voltage shift was observed from a low program voltage, 7 V. This is due to the high probability of electron tunneling through tunnel oxide, originating from the short potential barrier required for electron tunneling. Comparing Fig. 3a–c, an increased program voltage is required to bring enough threshold voltage shift as the tunnel oxide thickness increases. The maximum threshold voltage shift (ΔV_{th}) showed similar values of 3.46 and 3.71 V for the 30 and 40 Å tunnel oxide, respectively. When the 30 Å tunnel oxide is used, a threshold voltage change occurs during the C–V measurement since charge loss occurs easily due to defects in the oxide layer when the oxide is thin. These 30 and 40 Å tunnel oxide samples exhibit good program characteristics in 11 and 13 V, and require program operation times longer

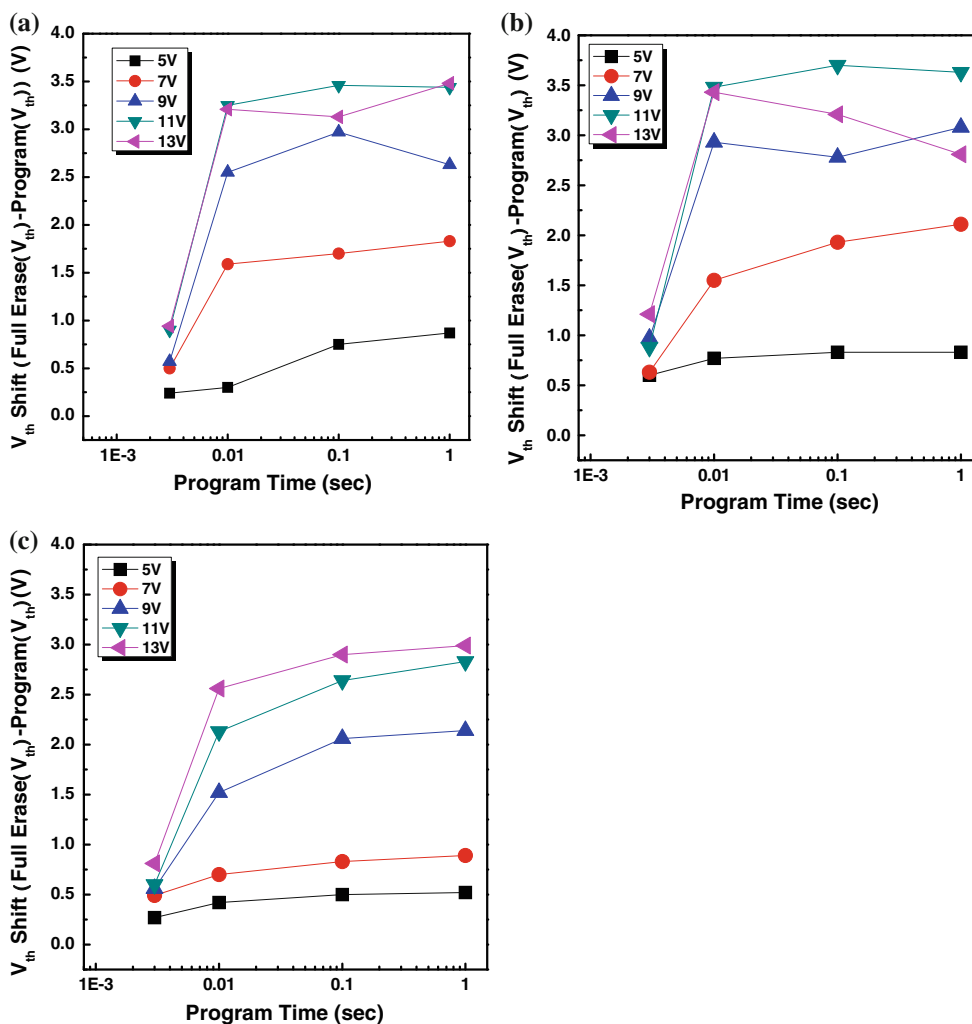


Fig. 3 Threshold voltage (V_{th}) shifts of **a** 30 Å, **b** 40 Å, **c** 50 Å tunnel oxide specimens after program pulse of 5–13 V and 3–1000 ms

than 10 ms. For the case of the 50 Å tunnel oxide sample, sufficient V_{th} shift did not occur during the program operation due to the decreased tunneling rate of electrons. Good program characteristics are shown at 11 V, 100 ms for the samples with 30 and 40 Å tunnel oxide, and at 13 V, 100 ms for 50 Å tunnel oxide sample. Hence, these conditions were used to program before evaluation of the erase characteristics.

Figure 4 shows threshold voltage shifts by erase pulses after programming, which are called memory windows. For the 30 and 40 Å tunnel oxides, satisfactory operation was carried out at -9 V or higher pulses. In the case of the 40 Å tunnel oxide, a maximum memory window of 3.4 V was recorded at -13 V for 100 ms. This value is lower than the case of a Si_3N_4 charge trap layer, which is known to be 5–6 V. Thus, lanthanum aluminate has a lower trap density than silicon nitride, but this value is considered large enough to distinguish data in a memory cell. For the 30 Å tunnel oxide sample, the memory window was lower

by 0.2 V relative to that of the 40 Å tunnel oxide, which is same as the program V_{th} difference. Hence, this memory window difference is due to the difference in charge loss shown in program characteristics. For a 50 Å tunnel oxide sample, gradual memory change is shown from -7 to -13 V, and the required time for the erase operation was longer than the other two samples. For all the samples, a generally larger voltage and longer time is required to erase in comparison with V_{th} shift after the program operation.

For the evaluation of reliability of the multilayer thin film memory structure, a program/erase cycling test was performed. For memory window measurements for the 30 and 40 Å tunnel oxide samples, the program and erase conditions were 11 V, 100 ms and -13 V, 100 ms, respectively. The same measurement for the 50 Å tunnel oxide sample used, a 13 V, 100 ms programming condition and a -13 V, 1000 ms erase condition. Measurement results after 10^4 cycles are shown in Fig. 5. The 30 Å tunnel oxide sample recorded about a 10% memory

Fig. 4 Memory windows of a 30 Å, b 40 Å, c 50 Å tunnel oxide specimen after erase pulse of -5 to -13 V and 3–1000 ms

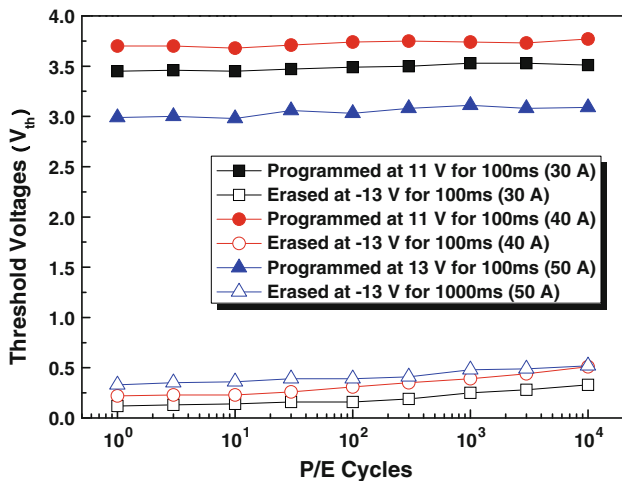
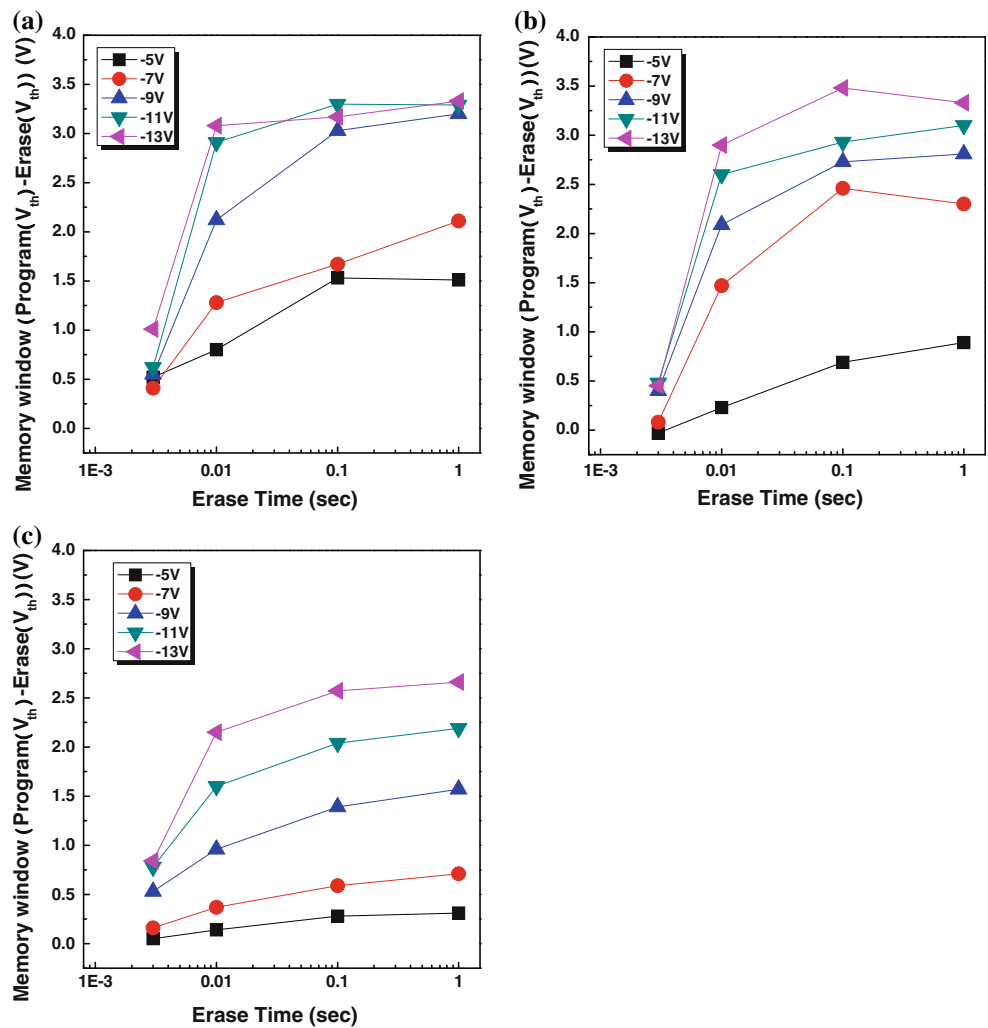


Fig. 5 Threshold voltage changes of Pt/Al₂O₃/LaAlO₃/SiO₂/Si capacitors after program/erase cycling test

window reduction after 3000 p/e (program/erase) cycles. If the tunnel oxide thickness is very thin, i.e., 30 Å, the tunnel oxide experiences a very large electric field of over

10 MV/cm due to the dielectric constant difference with LaAlO₃ and Al₂O₃. This can lead to the dielectric breakdown of silicon oxide, which has a dielectric strength of 8–10 MV/cm. In contrast, the 40 and 50 Å tunnel oxide samples showed a memory window reduction of 0.19 and 0.11 V after 10⁴ p/e cycles, which corresponds to 5.4 and 3.8% losses of initial memory windows. From these results, it is expected that 10⁵ cycles of operation, which is the standard for non-volatile memory reliability, will be available when a tunnel oxide thicker than 40 Å is used [11]. Furthermore, these structures have superior reliability compared to the SONOS structure which utilizes Si₃N₄ as charge trap layer [12].

Conclusion

Multilayer oxide film capacitor structures for non-volatile memory devices were fabricated and their structural properties and electrical characteristics were measured. To

perform program/erase operations with low power consumption and to minimize charge loss, aluminum oxide was utilized as the blocking oxide and lanthanum aluminate was used as the charge trap layer to replace silicon nitride. To observe memory characteristic difference by tunnel oxide thickness variation, multilayer structures with 30, 40, and 50 Å tunnel oxide were examined by pulse and C–V measurements. Maximum threshold voltage shift in the program and erase operation was observed when the 40 Å tunnel oxide was used. The program/erase cycling test for reliability measurement showed that the multilayer structure with the 30 Å tunnel oxide had the largest memory window reduction, which originated from repeated high electrical stress through the tunnel oxide. For 40 Å and thicker tunnel oxide samples, initial memory windows were sustained after 10^4 program/erase cycles. This result suggests that this Pt/Al₂O₃/LaAlO₃/SiO₂/Si structure can be used in next generation non-volatile memory without a reliability problem.

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